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09/801,608	03/08/2001	Lee Evan Eisen	AT9-98-538	5319

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EXAMINER	
TSAI, HENRY	

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Please find below and/or attached an Office communication concerning this application or proceeding.

PP9

Office Action Summary	Application No. 09/801,608	Applicant(s) EISEN ET AL.	
	Examiner Henry W.H. Tsai	Art Unit 2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 March 2001* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-48* is/are pending in the application.

4a) Of the above claim(s) *10-17, and 28-48* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9, and 18-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *10-17 and 28-48* are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *08 March 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _ .
4) ☐ Interview Summary (PTO-413) Paper No(s). ____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Election/Restrictions

1. This application contains claims directed to the following patentably distinct species of the claimed invention:

I. The species best illustrated by claims 1-9 and 18-27
II. The species best illustrated by claims 10-17 and 28-35
III. The species best illustrated by claims 36-48

Applicant is required under 35 U.S.C. 121 to elect a single disclosed species for prosecution on the merits to which the claims shall be restricted if no generic claim is finally held to be allowable. Currently, no claim is deemed generic.

2. During a telephone conversation with Mark E. McBurney on 3/29/04 a provisional election was made without traverse to prosecute the invention of species, claims 1-9 and 18-27. Affirmation of this election must be made by applicant in replying to this Office action. Claims 10-17, and 28-48 have been withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

3. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Drawings

4. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because in Fig. 7D,

reference characters "220"; "222"; "223"; and "224" each have been used to designate two different elements as shown in Figs. 2B and 2F.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to because

in Fig. 3A, reference No. 309, "CUR_LSptr" should read -CUR_LS_ptr-;

in Fig. 3B, reference Nos. 330, 331, 333, 337, 334 and 335, "CUR_LSptr" should read -CUR_LS_ptr-; reference No. 326, 328, 329, 336 "LStag" should read -LS_tag-; and

in Fig. 4B, reference Nos. 426, 428, 413, 431, 433, 434, 435, and 436, "LSptr" should read -LS_ptr-; reference 429, "OTQptr" should read -OTQ_ptr-; and similar problems exist in Figs. 4C-4G.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

6. The disclosure is objected to because of the following informalities:

at page 6, line 14, "FIGURES 2C-2D"; line 15, "FIGURES 2E-2G; line 19, "FIGURES 3B-3C; line 21, FIGURES 3D-3F; and

at page 7, line 3, FIGURES 4B-4D; and line 5, FIGURES 4E-4G each figure of them should be listed separately in Brief Description of the Drawings;

at page 12, line 21, "213" should read -211-; and

at page 16, line 16, "2D" should read -2E-.

Appropriate correction is required.

Claim Objections

7. Claims 3-5 and 20-22 are objected to because of the following informalities:

in claims 3 and 20, line 2, "an" should read -and-; and

in claims 4 and 21, it is unclear what is meant by "for a first type operation". It is suggested to change "for a first type operation" to -for the operation of said first type instruction-.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

8. Claims 1-9 and 18-27 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 1, it is not clear what the real claimed invention is since the step for the first type instruction (PUSH, 246, see Fig. 2C): "setting a first data value corresponding to a first

address stored in said link stack in a first portion of an entry in a queue having a plurality of entries" (see step 244 in Fig. 2C)) is also required for the second type instruction (POP, 249, see Fig. 2C); and the step for a second type instruction (POP, 249, see Fig. 2C): "setting said current value of said first pointer in a second portion of said entry in said queue" (step 251 see Fig. 2C) is also required for the first type instruction (PUSH, 246, see Fig. 2C). Similar problems exist in claim 18.

In claims 2 and 19, line 4, it is not clear which one is referred to as a second register. If it is the register in Operation Tracking Queue or link stack or somewhere in the system, then it should be clearly defined.

Claims 5 and 22, lines 2-3, "said second register in a said first portion of said entry" lacks proper antecedent basis since it was not defined previously.

In claims 8 and 25, lines 3-4, it is not clear how to compare said value from said retrieving step with a value from said second portion of said entry pointed to by said pointer value since said value from said retrieving step is an address (said second address, see claim 2, line 4) and a value from said second portion of said entry is a pointer value. Comparing an address with a pointer value was not described in the specification.

Applicant is required to review the claims and correct all language which does not comply with 35 U.S.C. § 112, second paragraph.

Claim Rejections - 35 USC § 102

9. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

10. Claims 1-9, and 18-27 are rejected under 35 U.S.C. 102(e) as being anticipated by Sinharoy (U.S. Patent No. 6,633,974) (hereafter designated as Sinharoy'974).

Referring to claim 1, Sinharoy'974 discloses, as claimed, a method for managing a link stack comprising the steps of: for a first type instruction (PUSH instruction see TABLE 1): setting a

first data value (Current Stack Operation 74, see Fig. 3C) corresponding to a first address (Return Address 68, see Fig. 3D) stored in said link stack (link stack 58, see Fig. 3B) in a first portion (Current Stack Operation 74, see Fig. 3C) of an entry (57, see Fig. 3C) in a queue (Branch Instruction Queue(BIQ) 56 see Fig. 3A2) having a plurality of entries (57, 57 see Fig. 3C); and for a second type instruction (POP instruction see TABLE 1): setting a current value of a first pointer (ptr1 in register 61b or ptr0 in register 61a, see Fig. 3B) into said link stack (link stack 58, see Fig. 3B) in a first register (register 61b when ptr1 is used or register 61a when ptr0 is used, see Fig. 3B); and setting said current value of said first pointer (ptr1 in register 61b or ptr0 in register 61a, see Fig. 3B) in a second portion (field 65 for ptro or field 67 for ptr1, see Fig. 3C) of said entry in said queue (Branch Instruction Queue(BIQ) 56 see Fig. 3A2).

Referring to claim 18, Sinharoy'974 discloses, as claimed, a data processing system comprising: a central processing unit (CPU) (10, see Fig. 1), said CPU including: a link stack (link stack 58, see Fig. 3B); and first logic (see Fig. 3A2 comprising such as current stack operation logic 81, curr_stack op 84, ptro control logic 89, and ptr1 control logic 91) operable for, for a first type instruction (PUSH instruction see TABLE 1): setting a

first data value (Current Stack Operation 74, see Fig. 3C) corresponding to a first address (Return Address 68, see Fig. 3D) stored in said link stack (link stack 58, see Fig. 3B) in a first portion (Current Stack Operation 74, see Fig. 3C) of an entry (57, see Fig. 3C) in a queue (Branch Instruction Queue(BIQ) 56 see Fig. 3A2) having a plurality of entries (57, 57 see Fig. 3C); and for a second type instruction (POP instruction see TABLE 1): setting a current value of a first pointer (ptr1 in register 61b or ptr0 in register 61a, see Fig. 3B) into said link stack (link stack 58, see Fig. 3B) in a first register (register 61b when ptr1 is used or register 61a when ptr0 is used, see Fig. 3B); and setting said current value of said first pointer (ptr1 in register 61b or ptr0 in register 61a, see Fig. 3B) in a second portion (field 65 for ptro or field 67 for ptr1, see Fig. 3C) of said entry in said queue (Branch Instruction Queue(BIQ) 56 see Fig. 3A2).

As to claims 2 and 19, Sinharoy'974 also, as best understood, discloses: the steps of for said second type instruction (POP instruction see TABLE 1), reading from said link stack (link stack 58, see Fig. 3B) a second address stored at a stack entry at said current value of said first pointer; and storing said second address in a second register (inherently in the Sinharoy'974's system such as the register 68 in the link

stack 66, see Fig. 3D; or Instruction register inside the CPU thereof).

As to claims 3 and 20, Sinharoy'974 also discloses: wherein said first type instruction is a "push" type instruction (PUSH instruction see TABLE 1) and said second type instruction is a "pop" type instruction (POP instruction see TABLE 1).

As to claims 4 and 21, Sinharoy'974 also discloses: further comprising the step of, for a first type operation (for the first type instruction (PUSH instruction see TABLE 1)), setting said first data value in a third register (the register for Current Stack Operation 74 see Fig. 3C).

As to claims 5 and 22, Sinharoy'974 also, as best understood, discloses: further comprising the step of, for third type instruction (such as FUSH instruction, see Col. 5, line 52-53), setting a second data value from said second register (inherently in the Sinharoy'974's system such as the register 68 in the link stack 66, see Fig. 3D; or Instruction register inside the CPU thereof) in a said first portion (the register 75a for predicted address see Fig. 3C)of said entry (57 in Branch Instruction Queue(BIQ) 56 see Fig. 3A2).

As to claims 6 and 23, Sinharoy'974 also discloses: said steps recited therein are performed in response to a fetch of a corresponding one of said first type instruction (PUSH

instruction see TABLE 1)and said second type instruction (POP instruction see TABLE 1).

As to claims 7 and 24, Sinharoy'974 also discloses: further comprising the steps of- receiving a pointer value in response to a pipeline flush, said pointer value operable for pointing into said queue (Note having pointer value operable for pointing into the Branch Instruction Queue(BIQ) 56 see Fig. 3A2 is an inherent step) ; and setting a current pointer value of said first pointer to a value in said second portion (field 65 for ptro or field 67 for ptr1, see Fig. 3C) of an entry pointed to by said pointer value.

As to claims 8 and 25, Sinharoy'974 also, as best understood, discloses: further comprising the steps of: retrieving a value from said second register (inherently in the Sinharoy'974's system such as the register 68 in the link stack 66, see Fig. 3D; or Instruction register inside the CPU thereof); and comparing said value from said retrieving step with a value from said second portion (field 65 for ptro or field 67 for ptr1, see Fig. 3C) of said entry pointed to by said pointer value.

As to claims 9 and 26, Sinharoy'974 also, as best understood, discloses: further comprising the steps of- in response to a compare in said comparing step, comparing said current value of said first pointer with a value in said first register; an in response to a compare of said current value of

said first pointer and said value in said first register, setting said value in said second register in said link stack at a location pointed to by said current value of said first pointer decremented by one (this is the inherent step such as that shown in TABLE 1, after the POP step in action 8, the counter 2 is decremented by one from 9 to 8).

As to claim 27, Sinharoy'974 also discloses: comprising system memory (RAM 14 see Fig. 1) coupled to said CPU (10, see Fig. 1), said system memory operable for storing a program of instructions including instructions of said first type (PUSH instruction see TABLE 1) and said second type (POP instruction see TABLE 1).

Conclusion

11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure, Scantlin'927 discloses a RISC architecture computer configured for emulation of a target computer which comprises a link stack as shown in fig. 8C; Rossbach et al.'999 also discloses a synchronizing link stack (LS 410) and the method for managing thereof; and Sinharoy'503 also discloses the link stack 58 and the method for

controlling the link stack corruption during speculative instruction branching similar to the claimed invention.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dr. Henry Tsai whose telephone number is (703) 308-7600. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:00 PM. If attempts to reach the examiner by telephone are unsuccessful, the examiner supervisor, Eddie Chan, can be reached on (703) 305-9712. Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the **TC 2100 receptionist whose telephone number is (703) 305-3900.**

13. In order to reduce pendency and avoid potential delays, Group 2100 is encouraging FAXing of responses to Office actions directly into

the Group at fax number: 703-872-9306.

This practice may be used for filing papers not requiring a fee. It may also be used for filing papers which require a fee by applicants who authorize charges to a PTO deposit account. Please identify the examiner and art unit at the top of your cover sheet. Papers submitted via FAX into Group 2100 will be promptly forward to the examiner.

HENRY W. H. TSAI
PRIMARY EXAMINER

April 1, 2004